VERTICAL-CONDUCTION AND PLANAR-STRUCTURE MOS DEVICE WITH A DOUBLE THICKNESS OF GATE OXIDE AND METHOD FOR REALIZING POWER VERTICAL MOS TRANSISTORS WITH IMPROVED STATIC AND DYNAMIC PERFORMANCES AND HIGH SCALING DOWN DENSITY

Abstract of the Disclosure

A vertical-conduction and planar-structure MOS device having a double thickness gate oxide includes a semiconductor substrate including spaced apart active areas in the semiconductor substrate and defining a JFET area therebetween. The JFET area also forms a channel between the spaced apart active areas. A gate oxide is on the semiconductor substrate and includes a first portion having a first thickness on the active areas and at a periphery of the JFET area, and a second portion having a second thickness on a central area of the JFET area. The second thickness is greater than the first thickness. The JFET area also includes an enrichment region under the second portion of the gate oxide.